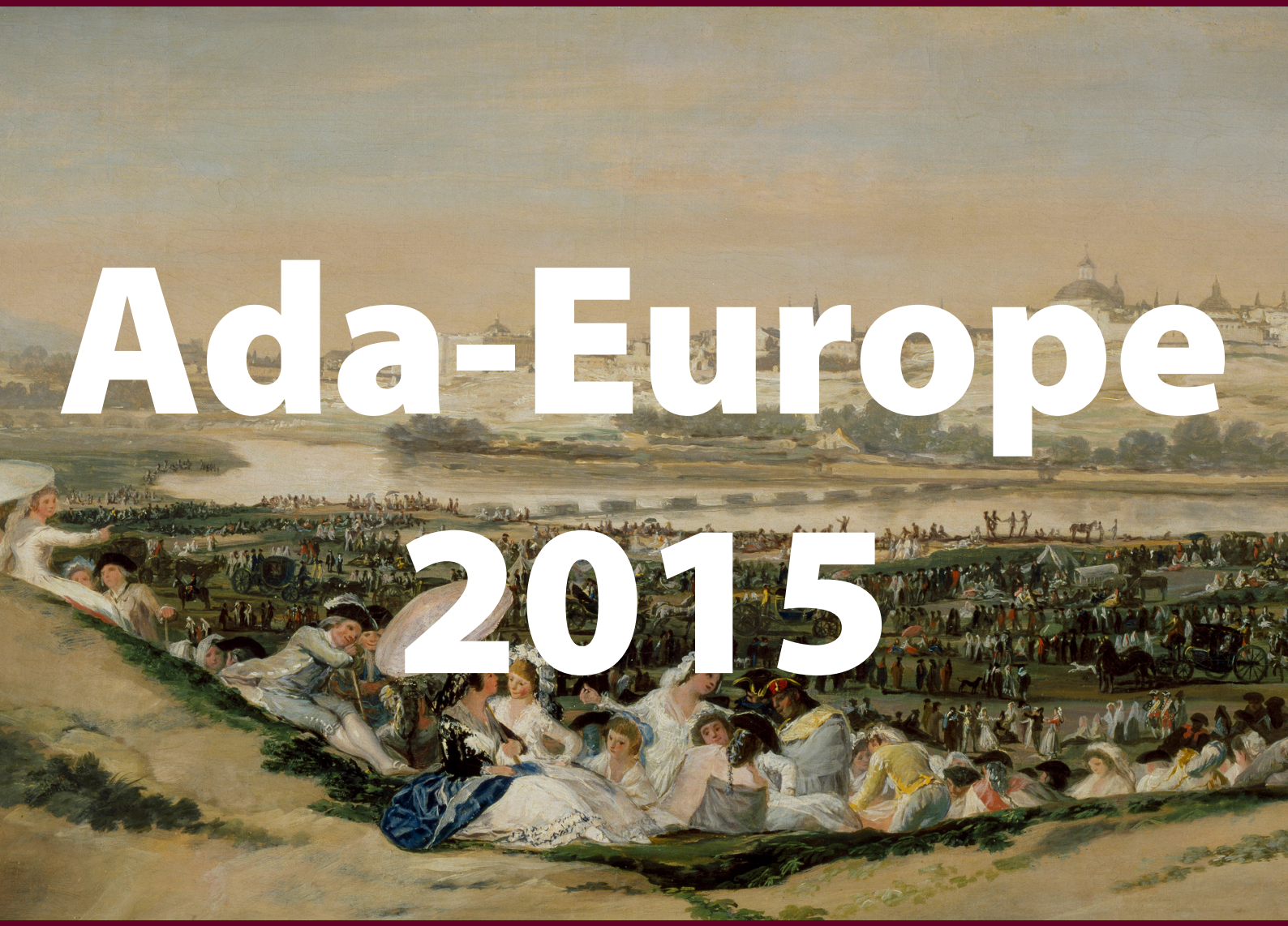
20TH International Conference on Reliable Software Technologies



Ada-Europe 2015

22-26 June 2015

Madrid, Spain

www.ada-europe.org/conference2015

Advance Program

Presentation

The 20th International Conference on Reliable Software Technologies – Ada-Europe 2015 will take place in Madrid, Spain. As per its traditional style, the conference will span a full week, with an ample offering of tutorials and satellite workshops on Monday and Friday, and a core program of scientific, industrial and technology talks on Tuesday to Thursday.

The conference will provide an international forum for researchers, developers and users of reliable software technologies all over the world. Presentations and discussions cover applied and theoretical work currently conducted to support the development and maintenance of reliable software systems.

Madrid is the capital city of Spain as well as a technology and industry centre, where a high number of leading industries and research institutes are located. It is also one of the top visiting places in Europe, with a rich legacy of art and historical buildings, and a lively environment for shopping, eating, and nightlife.

The proceedings will be published by Springer in "Lecture Notes in Computer Science (LNCS)", volume 9111.

Overview of the Week

Monday	Tuesday	Wednesday	Thursday	Friday
	Opening /Welcome			
Tutorials & De-CPS Workshop	Keynote Talk **Certification of Mixed-Criticality Systems**	Keynote Talk **Safety-Critical Railway Systems**	Keynote Talk **Philae Lander On-board Computer**	**Tutorials & ACVI Workshop**
	Regular Session **Language Technology**	Industrial Session **Critical Systems**	Regular Session **Critical Systems**	
	Vendor Session	Regular Session **Real-Time Applications**	Industrial Session **Tools at Work**	
	Industrial Session **Ada Applications**	Special Session **Advances on Methods**	Regular Session **Multicore & Distributed Systems**	
	Ada-Europe General Assembly Welcome Cocktail	Conference Banquet Best Paper Award	Best Presentation Award Closing Session	

Keynote Talks

IEC-61508 Certification of Mixed-Criticality Systems Based on Multicore and Partitioning

Jon Pérez

IK4-IKERLAN

Tuesday, June 23rd at 9:30

Abstract

The development of mixed-criticality systems that integrate applications of different criticality levels (safety, security and real-time) may allow for considerable cost-size-weight reduction, for increased reliability and capacity for scaling. However, this very same integration poses several important challenges with respect to current safety certification standards. This keynote presents a safety concept for a SIL3 fail-safe wind turbine mixed-criticality control system based on COTS multicore partitioning that complies with IEC-61508, a cross-domain reference safety standard. The safety concept has been positively assessed by a certification body.

Presenter

Dr. Jon Pérez is head of the embedded systems research line at IKERLAN, working on the design and development of safety-critical embedded systems, for example SIL4 railway signaling (ERTMS/ETCS). He is a certified TÜV Functional Safety engineer for the design of hardware and software based on the IEC-61508 standard. He has received a B. Eng in Industrial and Robotics at Mondragon University, a M.Sc. in Electronics & Electrical Engineering with distinction at the University of Glasgow and he finished his doctoral studies in Computer Science at Technische Universitaet Wien (TU Wien) in the field of safety-critical embedded systems.

Software Development of Safety-Critical Railway Systems

Javier Rodríguez

Siemens Rail Automation

Wednesday, June 24th at 9:30

Abstract

The strong rise of the railway sector in the last decade of the 20th century created the need for more complex systems with greater safety, reliability, availability, and maintainability requirements. In order to help with the definition and performance of these systems, various European standards have been defined with the participation of both technology companies and operators. The CENELEC 50128 is one of the standards that regulate the development of software for railway control and protection systems.

This keynote presents a strategy defined by the Research & Development department at Siemens Rail Automation to develop the majority of its safety-critical systems in order to achieve conformance with this standard by reviewing all the life-cycle of the software.

Presenter

Mr. Javier Rodríguez is currently responsible for Mass Transit ATP systems in the Research and Development department at Siemens Rail Automation. During two decades he has been participating as software engineer, system engineer, and project manager in the definition, specification, development, implementation, verification, and validation of real-time safety-critical embedded systems fulfilling the CENELEC standard defined for these systems. He graduated as a Telecommunication Engineer at the Technical University of Madrid (UPM) in 1995, and is certified in Software Testing by the British Computer Society.

Parque del Retiro

The Central On-board Computer of the Philae Lander in the Context of the Rosetta Space Mission

Andras Balazs

Wigner Research Centre for Physics

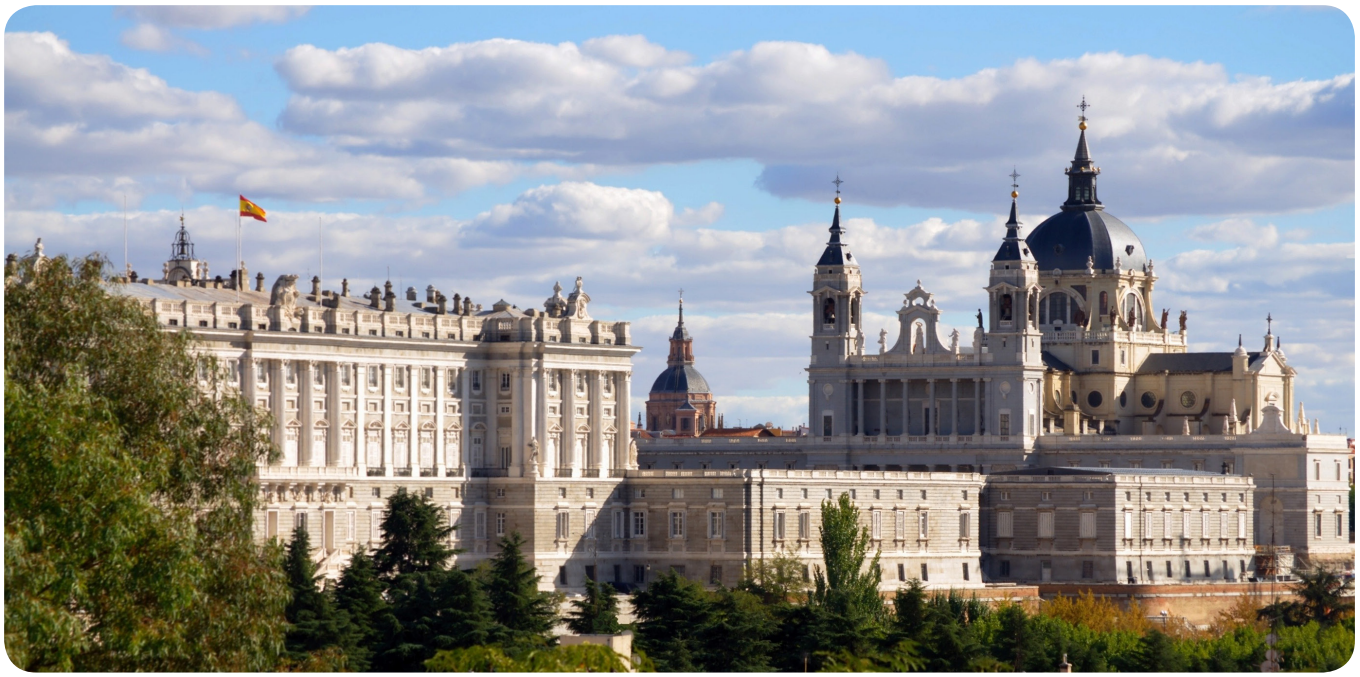
Thursday, June 25th at 9:30

Abstract

The Rosetta-Philae space mission is an unprecedented venture. After a ten-year journey across the Solar System and many complicated manoeuvres, the Rosetta spacecraft smoothly approached a small (2-4 km in diameter) celestial body, comet CG/67P. Furthermore, the spacecraft executed additional fine manoeuvres to fly a multitude of low and high altitude orbits around the comet, mapping its shape and surface in detail never seen before, and has continued to observe it for a year since then. The Rosetta spacecraft is equipped with scientific instruments that deliver a wealth of new knowledge about the CG/67P comet, in addition to spectacular pictures. Delivering the Philae lander onto the surface of the comet 500 million km away from Earth was also a remarkable technological success. The direct measurements made by the Philae lander on the surface of the comet provided significant new knowledge. The first half of the talk gives a brief overview of the objectives and highlights of the Rosetta-Philae mission. In the other part of the talk the major hardware and software design aspects, including the conceptual design and implementation of the central on-board computer (CDMS) of the Philae lander are outlined. This will illustrate the implementation of fault tolerance, autonomous operation and operational flexibility by means of specific linked data structures and code execution mechanisms that can be interpreted as a kind of object-oriented model for mission sequencing.

Presenter

Andras Balazs graduated from the Faculty of Electrical Engineering at the Technical University of Budapest in 1982. Since then - with two temporary interruptions - he has been working for the Space Physics and Technology Department at KFKI Research Institute for Particle and Nuclear Physics (now Wigner Research Centre for Physics), Budapest, Hungary, as a research, hardware and software engineer. Between 1989 and 1990 he worked for the Max Planck Institut für Extraterrestrische Physik, Garching/Munich, Germany. Between 2003 and 2010 he worked for the Deutsches Zentrum für Luft- und Raumfahrt, Cologne, Germany. During the past three decades he has participated as hardware and software system designer of flight and ground support equipment, either as team member or team leader in numerous space projects such as: Venus-Halley, Freja, Mars-Phobos, Spectrum X-ray Gamma, Mars-96 and Rosetta-Philae. He prepared the conceptual hardware and software design of the fault tolerant central on-board computer of the Philae lander, led and contributed to the implementation, supported its testing, validation and operation in space. He has more than 40 publications.



Palacio Real

Tutorials

Access Types and Memory Management in Ada 2012

Jean-Pierre Rosen

Monday, June 22nd at 9:30

In most languages, pointers are either low-level (pure hardware addresses in C), or implicit (Java, C#).
Ada provides explicit pointers, but of a higher level of abstraction (hence the use of the term "access"), disconnected from the hardware level, and as safe as possible. In addition, the language includes sophisticated features for controlling memory allocation and deallocation. While this has great benefits, it may confuse those who are used to pointers in other languages. Proper usage also requires some difficult to grasp notions, like accessibility levels. This tutorial explains all the issues with Ada access types, from basic usage to sophisticated features like remote access types. Many practical examples demonstrate how to use them and how to control memory allocation, and special emphasis is provided for the latest features offered by Ada 2005 and 2012. A must-attend for all those using access types.

Reasons for attending

- Understand what makes Ada access types different from other languages' pointers.
- Explore rarely taught issues, like accessibility levels, storage pools and subpools, remote access types...
- Learn when and how to use access types and when not to use them.

Level

Intermediate. Expected audience experience: Casual knowledge of Ada.

Designing and Checking Coding Standards for Ada

Jean-Pierre Rosen

Monday, June 22nd at 14:30

Most companies have developed coding standards (often because having one is a requirement for certification), but few have conducted a real analysis of the value, consistency, and efficiency of the coding standard.
This tutorial presents the challenges of establishing a coding standard, not just for the sake of having one, but with the goal of actually improving the quality of software. This implies not only having "good" rules, but also having rules that are understood, accepted, and adhered to by the programming team.
The issues of automatically checking the rules is also fundamental: experience shows that no manual checking can cover the programming rules to a satisfactory extent. The tutorial presents the tools available, and criteria for choosing such a tool.
This tutorial is an update of the one given at previous Ada-Europe conferences.

Reasons for attending

- Understand the value of coding standards.
- Learn how to choose you own coding rules, in a way that is both useful and efficient.
- Consider the difficulties and pitfalls of introducing coding standard to the development teams, and how to overcome them.

Level

Intermediate. Expected audience experience: No special requirement

Presenter

Jean-Pierre Rosen is a professional teacher, teaching Ada (since 1979, it was preliminary Ada!), methods, and software engineering. He runs Adalog, a company specialized in providing training, consultancy, and services in all areas connected to the Ada language and software engineering. He is chairman of AFNOR's (French standardization body) Ada group, AFNOR's spokesperson at WG9, member of the Vulnerabilities group of WG9, and chairman of Ada-France. Adalog offers regularly on-site and off-site training sessions in Ada. This tutorial is based in part on the "advanced Ada" course offered by Adalog.

Parallelism in Ada, Today and Tomorrow

Brad Moore and Stephen Michell

Monday, June 22nd at 9:30

Since inception, the Ada programming language has supported concurrency and parallelism. A task in Ada provides excellent support for course grained parallelism, but with the advent of multicore technologies, finer grained parallelism solutions are now desired that make it easier to spread the workload across the available cores. This tutorial takes a hands-on approach to explore available solutions that work in Ada today, using the Paraffin open source libraries. Topics covered include: Divide and Conquer problems, load balancing strategies

including Work Stealing, Work Sharing, Work Seeking, parallel loops, parallel recursion, parallel blocks, executor pools, reductions, synchronization, real-time parallelism, Ravenscar compliancy, oversubscription avoidance, and strategies for determining where best to inject parallelism.

The tutorial will provide examples to work through, which attendees can use to further their understanding of the concepts. Attendees may also find it interesting to compare their performance results from different operating systems and platforms. The tutorial then explores how syntax proposals being considered for Ada 202x could further simplify how one could express parallelism in their source code. This part of the discussion will describe the notion of tasklets, and also describe how the tasklet model can be applied to tie the proposed syntax to the implementation behaviour to support general and real-time systems.

The morning session will focus on a quick review of the parallelism and concurrency features built into the Ada 2012 standard, followed by how the Paraffin libraries may be applied to achieve fine-grained parallelism. Various examples and problems will be worked through, which will continue into the afternoon session. The afternoon will conclude by examining the future proposals for parallelism in Ada 202X.

Reasons for attending

The attendees will become familiar with divide and conquer parallelism, and how it can be applied in their Ada 2005 and Ada 2012 programs. Attendees will learn how to choose an optimal strategy for a given parallelism opportunity, and develop a better understanding of the effects of various controls and inputs to the parallelism.

Level

The tutorial material is targeted for an intermediate level of understanding of multicore computing, and the Ada programming language. Familiarity with these topics is helpful, but not essential. Ada 2005 and Ada 2012 features will be used during the presentation but attendees will not need to be familiar with those features, since they are not fundamental to the concepts being presented. The material should be of interest to anyone seeking to improve performance of their code on multicore platforms, and make better use of the available processing resources to solve problems.

Presenters

Brad Moore works as a software engineer at General Dynamics Canada developing communication systems for military use. A long time user of Ada, he became involved with ISO/IEC JTC1/SC22/WG9, the working group maintaining the Ada standard, during the Ada 2005 standardization process, when he also joined the Ada Rapporteur Group (ARG). Since then he has been involved with WG9 and the ARG in the work associated with producing the Ada 2012 version of the standard. He also has been involved in the real-time community for Ada and has participated in recent IRTAW workshops. In 2009, he happened to attend a parallelism conference where a paper was presented entitled "Reducers and other Cilk++ Hyperobjects". This presentation ignited an interest in parallelism, which led to the development of the Paraffin libraries for Ada. Since then, Brad has been involved in several papers and presentations on the topic of parallelism in Ada. Brad and Steve form part of the gang of four currently developing parallelism proposals to be considered for a future revision of the Ada, standard informally known as Ada 202x. Brad holds a BSc from the University of Calgary, Canada.

Stephen Michell has been a contributing member of the Ada community for more than 30 years. He has concentrated on the safety, security and concurrency aspects of Ada through most of this time. He implemented Ada83 on a multiprocessor platform, was a distinguished reviewer for Ada 9X, authored the initial Guidance for the use of Ada in high integrity systems, helped to develop the Ravenscar Tasking Profile, and is developing proposals for parallelism in Ada. Stephen is also deeply involved in the standardization of programming languages at the international level, chairing the Canadian mirror committee to ISO/IEC JTC1/SC22 Programming Languages subcommittee and convening ISO/IEC JTC1/SC22/WG23 Programming Language Vulnerabilities working group. Stephen holds a BS Mathematics from the University of Waterloo, Canada, and a MSc in Mathematics and Systems Engineering from Carleton University, Canada.

Probabilistic Timing Analysis

Francisco J. Cazorla, Tullio Vardanega, Jaume Abella and Mark Pearce

Monday, June 22nd at 9:30

The market for Critical Real-Time Embedded Systems (CRTES) is experiencing an unprecedented growth. The inclusion in CRTES of increasingly sophisticated value-added functions, such as for example Advanced Driver Assistance Systems, causes CRTES makers to continue to seek increasingly more guaranteed computation performance. CRTES designers also consider mixed-criticality solutions so that more functional value can be obtained per unit of product. Probabilistic techniques may greatly aid in this regard. In particular, with Measurement-Based Probabilistic Timing Analysis (MBPTA) methods the execution time of the application can be accurately modelled – at some level of execution granularity – by a probability distribution. MBPTA seeks to determine worst-case execution time (WCET) estimates for arbitrarily low probabilities of exceedance, termed probabilistic WCET or pWCET. Even if any pWCET may in principle be exceeded, this can only happen with a given probability, which can be determined at a level low enough for the application

domain; for example, in the region of 10-15 per hour of operation, largely below the acceptable probability of failure in certified systems.

In the last few years, probabilistic timing analysis (PTA) in general, and MBPTA in particular, has emerged as a viable alternative to classic timing analysis approaches. Owing to its observation-based nature, MBPTA requires considerably less information on the detailed internal behaviour of the hardware and the software of the system, which is instead the crux of classic WCET methods. PTA has become an acknowledged area of scientific interest with an increasing number of active researchers and a good and rising score of publications. As a testimony to that, the last 2 RTSS editions (2012 and 2013) have had 1 paper in PTA and ECRTS 2014 has 4 papers on PTA related topics and a specific session on Probabilistic Methods. Furthermore, the Best Paper Award in the DAC 2014conference went to a PTA-related paper. There also is high industrial interest on PTA, sensed via direct and indirect participation in the PROXIMA project, which focuses on furthering PTA methods and technology for multicore and manycore processors.

This tutorial introduces attendees to Measurement-Based Probabilistic Timing Analysis (MBPTA) with emphasis on its properties from the end user point of view and its requirements on the underlying hardware and software platform. Through didactic material and several examples, the audience will be exposed to understanding MBPTA concepts. The tutorial also presents the current advances of MBPTA and the main challenges it has to address to be increasingly used by industry.

The tutorial will consist on two main parts: An introductory part to PTA and MBPTA and a hands-on session.

The morning introductory session will cover the basics of PTA as well as the latest techniques on PTA:

- Introduction to PTA technology
- PTA bottom-up:
  - PTA-enabling hardware designs
  - PTA-enabling software designs
- Challenges in deriving pWCET estimates on COTS processors
- The case of cache memories
- Conclusions and outlook

Afternoon hands-on session: We will carry out a set of exercises using PTA tools so that the audience can get hands-on experience with PTA techniques and technology. To that end, the attendees will be provided a virtual machine to be run in their laptop on which experiments will be carried out.

Each attendant is required to have a laptop with a standard Linux or Windows distributions. They will be provided a virtual machine with a set of preinstalled PTA tools.

Reasons for attending

The envisioned tutorial will cause benefits in two directions:

- Introducing researchers and industrial practitioners to the PTA requirements, benefits, and basic functioning. With PTA acknowledged as a fertile area of research, this part of the tutorial will allow participants to catch up with the essentials of PTA faster and to a greater depth.
- Expose participants to the latest advances in PTA for method, techniques and requirements on the hardware and the software of the system, with a view to how they compare to other techniques in the state of the art

Level

The tutorial has an introductory level. The audience should have basic knowledge on real-time systems and be familiar with basic concepts of WCET analysis, knowing the basic difference between static and measurement-based timing analysis. No prior knowledge on PTA is required.

Presenters

Francisco J. Cazorla is the leader of the CAOS research group at BSC and researcher in the Spanish National Research Council (IIIA-CSIC). Francisco has led several bilateral projects with industry: IBM, Sun Microsystems (now Oracle) and the European Space Agency. He also currently leads the PROXIMA FP7 STREP EU project. He has three submitted patents on the area of hard-real time systems. His research area focuses on multithreaded architectures for both high-performance and real-time systems on which he is co-advising ten PhD theses. He has co-authored over 80 papers in international refereed conferences. He spent five months as intern in IBM‘s T.J. Watson in New York in 2004.

Tullio Vardanega is at the University of Padua, Italy, since January 2002. He holds a master degree in Computer Science from the University of Pisa, Italy, and a PhD in Computer Science from the Technical University of Delft, Netherlands. He worked at European Space Agency Research and Technology Center from July 1991 to December 2001. At the University of Padua, he teaches and leads research in the areas of high-integrity distributed real-time systems and advanced software engineering methods. He has a vast network of national and international research collaborations. He has co-authored 90+ refereed papers and held organizational roles in several international events and bodies, for ESA, the European Commission, ISO, IEEE and Ada-Europe.

Jaume Abella is a senior PhD. Researcher in the CAOS group at BSC and member of HIPEAC. He worked at the Intel Barcelona Research Center from 2005 to 2009 in the low-level design and modelling of circuits and microarchitectures for fault-tolerance and low power, and led the group on memory hierarchies. Jaume authored 15 patents at Intel. He joined the BSC in 2009 where he is in charge of hardware designs for FP7 PROXIMA, BSC certification activities in VeTeSS, and involved in H2020 SAFURE and two ESA projects. He has authored more than 80 papers in top conferences and journals in the area. He has advised 6 PhD/master

students and is co-advisor of 7 PhD/master students.

Mark Pearce is a Software Engineering specialist working with Rapita Systems Limited. He is currently actively involved in a number of research and development projects developing probabilistic timing analysis techniques and other timing solutions for multi-core architectures. Prior to this, he has gained extensive experience working on complex embedded real-time systems in a number of industry sectors including aerospace, defence and manufacturing. Whilst developing broad experience across the entire software life cycle, he has also specialized in the area of testing and integration. Mark gained a B.Eng degree studying Microelecronics and Microprocessor Applications and an MBA through study at Henley Management College.

Ada 2012 (Sub)Type and Subprogram Contracts in Practice

Jacob Sparre Andersen

Friday, June 26nd at 9:30

One of the important, new features in Ada 2012 is a streamlined support for contract-based programming with "contract aspects". They allow the programmer to specify even more details about types and subprograms in a formal and testable form. If used carefully, they can make package specifications easier to read, and help identifying use and implementation errors faster.

To really make sense, it is important that the contract aspects are applied in a consistent way. The goal of this tutorial is to help the programmer in that direction. It is organised in three sections: An introduction to Ada 2012 contract aspects. Guidance on how one can ensure a consistent application of contract aspects across a whole package. And finally a guided, practical exercise in applying contract aspects.

Reasons for attending

The tutorial will give the participants guidance and practical exercises in applying contract aspects consistently across a set of (sub)types and subprograms. The tutorial is intended to prepare existing Ada programmers for using Ada 2012 contract aspects in future projects.

Level

The tutorial is intended to be on an intermediate level. The intended audience is software engineers, who already know Ada, but have not yet used the "programming by contract" aspects added in Ada 2012. It is advised that the attendees bring laptops with an Ada 2012 compiler installed, even if the practical exercises can be worked through with pen and paper.

Presenter

Jacob Sparre Andersen has previously given talks and tutorials on the use of Ada 2012 for contract-based programming at Ada-Europe 2013, DANSAS'13, FOSDEM 2014, Ada-Europe 2014, Linux-Day/ Cagliari 2014 and FOSDEM 2015. He has previously taught on courses in physics, mathematics, statistics, software engineering (and financial instruments). Jacob Sparre Andersen runs his own consulting company in Hørsholm, Denmark. See http: //www.jacob-sparre.dk/ cv/ for a full curriculum vitae.

When Ada Meets Python: Extensibility through Scripting

Emmanuel Briot and Ben Brosgol

Friday, June 26nd at 14:30

Python, like many scripting languages, lends itself quite well to controlling or working cooperatively with applications written in other languages; in so doing it allows such applications to be customized or extended by their users.

In the first part of this tutorial we will summarize the main elements of the Python language and describe the consequences of Python's dynamic typing, its memory management mechanism, and related topics. In the second part we will explain how Python code can be integrated into existing Ada applications (without recompiling) through a freely available API in the GNAT Components Collections (GNATColl.Scripts) and then discuss specific usage scenarios. We will show how GNATColl.Scripts is used for extensibility in the GNAT Programming Studio (GPS) IDE and will also summarize how to use Python in connection with gdb and pretty printers.

Reasons for attending

Attendees will learn how to exploit the benefits of a scripting language in conjunction with Ada, in particular how to use Python to extend existing applications with new functionality.

Level

Intermediate level. Attendees should be familiar with Ada 95 or a more recent version of the language standard. Knowledge of Python is not required.

Presenters

Emmanuel Briot has been with AdaCore since 1998. He has been involved in a variety of projects, in particular oriented towards graphical user interfaces, including GtkAda, GPS, XML/Ada, the GNAT Components Collection, GNATtracker, and AdaCore's internal Customer Relations Management tool. He holds an engineering degree from the Ecole Nationale des

Telecommunications (Brest, France).

Dr. Benjamin Brosgol joined AdaCore in 2000 and is a senior member of the technical staff. He has been involved with programming language design and implementation for more than 30 years, concentrating on languages and technologies for high-integrity systems. He participated in the design of Ada 83 and Ada 95, and he was a member of the Expert Group for the Real-Time Specification for Java. Dr. Brosgol holds a BA in Mathematics from Amherst College, and MS and PhD degrees in Applied Mathematics from Harvard University.

Software Measures for Dependable Software Systems

William Bail

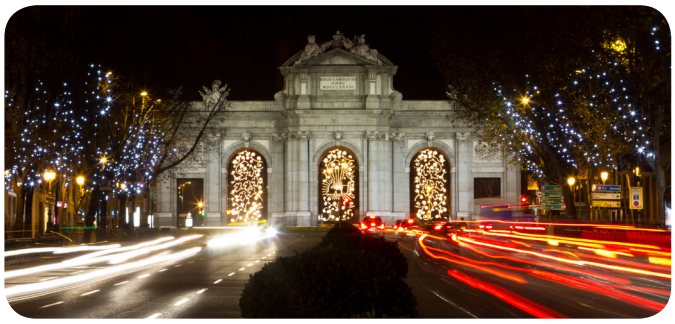
Friday, June 26nd at 14:30

Software measurement is a key practice in software development, allowing developers to monitor the emerging attributes of the software product as well as the processes used to develop the product. Such monitoring is crucial in order to achieve the desired attributes of the system and avoid surprises late in the system development, which would negatively affect cost and quality. The exercise of proper and appropriate software measurement can assist in this goal. One key is to select and apply the right measures, and to avoid those that do not provide useful information. There is a temptation to collect many metrics with the idea that more data is better. Such a collection strategy results in wasted effort and at times misleading indicators such as false positives and false negatives.

This tutorial surveys the range of popular and effective measures, and provides guidelines for their selection, application, and interpretation. It provides an assessment of the utility of many popular measures, and makes recommendations for effective subsets that provide cost-effective feedback and predictive information.

Level

Intermediate. The target audience should be familiar with software development and code construction, as well as aspects of software management. Attendees should have at least 2 years experience in software development, involving hands-on experience in software measurement



Puerta de Alcalá

Software Design Concepts and Pitfalls

William Bail

Friday, June 26nd at 9:30

Software design is a key activity in overall software development - without some aspect of design, SW development cannot take place.. Software design is tightly intertwined with the requirements engineering process. Understanding its concepts and principles is essential to being able to develop large, dependable software systems. It is also important to understand how design relates to the other development activities.

This tutorial will present a perspective of design and provide the framework within which software design efforts can be formed. This tutorial will not provide in-depth analysis of all facets of design due to time limitations. The design of software involves the transformation of the system's requirements into an arrangement of components whose interactions will satisfy the allocated requirements. All designs have inherent properties, with not all designs having the same properties, resulting in a need to select a design for a system that is coherent with the system's intended role and usage profile. In addition, there are commonly-used design patterns selected for their properties, but some patterns are less effective, creating pitfalls.

The tutorial will examine the core concepts of software design and architecture, and explain how design relates to the requirements assigned to the system. It will discuss design-related standards and present some design quality attributes which need to be assessed as systems undergo the design process. In addition, the tutorial will provide some examples of good and faulty design. The tutorial will also discuss unsolved areas of design and areas where research is needed to fill in gaps in knowledge. The tutorial will describe the SWEBOK view of design and how it relates to the information being presented.

Reasons for attending

The tutorial will present a perspective of design and provide the framework within which software design efforts can be formed. It will provide practical guidance on how to approach a design effort, and will give insight into detecting design qualities. It will also provide some trade-offs in selecting design techniques. The tutorial will discuss issues and challenges commonly encountered in development projects today, and will describe some heuristics in overcoming the risks inherent in these challenges.

Level

Intermediate, with the target audience being those practitioners responsible for creating a design for software systems.

Presenter

Since 1990, **Dr. Bail** has worked for The MITRE Corporation in McLean VA as a Computer Scientist in the Software Engineering Center (SWEC). MITRE is a not-for-profit corporation chartered to provide systems engineering services to the U.S. Government agencies, primarily the DoD, the FAA, and the IRS. Within MITRE, the SWEC focuses on supporting various programs with consultation, particularly transitioning emerging technologies into practice. He has written software measurement policy and guidance for multiple customers. Dr. Bail's technical areas of focus include dependable software design and assessment, metric definition and application, error handling policies, techniques for software specification development, design methodologies, metric definition and application, and verification and validation.

Prior to 1990, Dr. Bail worked at Intermetrics Inc. in Bethesda MD. From 1989 to 2011, he served as a part-time Adjunct Professor at the University of Maryland University College where he develops instructional materials and teaches courses in software engineering, in topics such as Software Requirements, Verification and Validation, Software Design, Software Engineering, Fault Tolerant Software, and others. Previously, Dr. Bail taught part-time at The University of Maryland from 1983-1986 in the Computer Science Department for undergraduate courses in discrete mathematics, computer architecture, and programming language theory. Dr. Bail has presented tutorials on Cleanroom Software Engineering, Semi-Formal Development Techniques, Statistical Testing, and Requirements Engineering for Dependable Systems at SIGAda, Ada-Europe, NDIA Systems Engineering Conference, and other conferences. Dr. Bail received a BS in Mathematics from Carnegie Institute of Technology, and a MS and Ph.D. in Computer Science from the University of Maryland.

Real-time / Embedded Programming with Ada 2012

Patrick Rogers

Friday, June 26nd at 9:30

We present both a tutorial and a developer workshop based on the tutorial material.

The tutorial covers the use of Ada in programming real-time and/or embedded systems. We focus on the facilities provided to developers for use at the application level, but also cover the required run-time library semantics. Hence there are four major sections: the language facilities for embedded systems programming, the standard run-time library support for analyzing and meeting hard deadlines, the application-level packages and pragmas defined in the Real-Time Annex for applications with hard deadlines, and the Ravenscar Profile. The focus is on the rationale and expected usage of the facilities, with extensive examples.

The developer workshop allows the student to put some of the material learned in the tutorial section into practice using an ARM-based embedded target platform providing a Ravenscar-compliant run-time environment. AdaCore will provide an Ada 2012 tool-chain and several ARM-based target boards. Students may keep both the tools and ARM board at the end of the day, if they wish. (Students must provide their own computers having at least one USB port and the ability to run Windows either natively or in a virtual machine.)

Reasons for attending

Developers will understand the unmatched real-time programming facilities provided by Ada. In addition, the low-level programming facilities, so often misunderstood, are covered in detail. The hand-on developer's workshop will make these facilities concrete.

Level

This tutorial is intended for developers familiar with some of the more advanced features of Ada, including tasking and access types. Hence it is an upper-intermediate to advanced tutorial. Prior experience in the real-time and embedded programming domains is not required but is obviously helpful.

Presenter

Patrick Rogers is product manager for bare-board systems and a Senior Member of the Technical Staff with Ada Core Technologies, specializing in high-integrity and real-time application support. A computing professional since 1975 and an Ada developer since 1980, he has extensive experience in real-time applications in both embedded bare-board and POSIX-based environments. An experienced lecturer and trainer since 1981, he has provided numerous tutorials and courses in real-time programming, software fault tolerance, hard real-time schedulability analysis, object-oriented programming, and the Ada programming language. He holds B.S. and M.S. degrees in computer science from the University of Houston and a Ph.D. in computer science from the University of York, England, as a member of the Real-Time Systems Research Group.

Plaza Mayor

Workshops

Challenges and new Approaches for Dependable and Cyber-Physical Systems Engineering (De-CPS 2015)

Monday, June 22nd at 9:30

Domain and topics

From the USA to Europe, there is a crescendo of industrial and research interest in Cyber-Physical Systems (CPS). One distinguishing trait of CPS is that they integrate software control and decision making with signals from an uncertain and dynamic environment. CPS often involve heterogeneous and hierarchical systems, and their design makes extensive use of models. The Horizon 2020 program framework of the European Union devotes considerable attention in the current work program to various challenges associated with developing, integrating and providing assurance concerning CPS.

The workshop will gather together industrial practitioners and researchers concerned with dependable and Cyber-Physical Systems engineering, and use the momentum provided by the 20th International Conference on Reliable Software Technologies to foster further collaborative initiatives.

We promote gender equality in research and innovation. The strength-in-depth represented by the female scientists in our team will hopefully inspire a new generation of women to pursue an interest in science as a career. Some of the expected impact of the H2020 are:

- Increase the participation of women in research, improve their careers and achieve gender balance in decision making,
- Increase the scientific quality and societal relevance of produced knowledge, technologies and innovations by integrating an in-depth understanding of both genders needs, behaviours and attitudes. It also contributes to the production of goods and services better suited to potential markets.

The topics addressed by the workshop include the following:

- Industrial challenges and experience reports on co-engineering for multiple dependability concerns in CPS engineering.
- Modeling and analysis of Cyber-Physical Systems (CPS) via contract-based approaches
- Tools and methodologies to guarantee safety-related properties, including real-time and mixed-criticality cohabitation
- Challenges posed for CPS design and safety verification by multi-core processors.

Important dates and instructions to authors

Authors are invited to submit a position paper of 2 to 4 pages in length in a conference-style format of choice to the author at the following submission page https://easychair.org/conferences/?conf=decps2015. The authors of accepted papers will be invited to publish an extended version of their contribution in the Ada-User Journal after the end of the workshop.

- Submission deadline: April 4th.
- Notification to authors: May 12th.
- Workshop : June 22th, Madrid, Spain
- After-workshop final version: September 15th.
- Publication: December 2015

Organizing and program committee

Scientific and Industrial Steering Committee

- *Katrina Attwood*, University of York, UK.
- *Alessandra Bagnato*, SOFTEAM, France.
- *Daniela Cancila*, CEA LIST, France.
- *Philippa Ryan Conmy*, Rapita Systems, UK.
- *Laila Gide*, Director for Advanced Studies Europe, reporting directly to Thales CTO – Technical Directorate THALES, France.
- *Silvia Mazzini*, INTECS, Italy.
- *Pavithra Prabhakar*, IMDEA, Spain.
- *Alejandra Ruiz*, Tecnalia, Spain.

Honorary Chair

- *Antoine B. Rauzy*, Director of the Chair Blériot-Fabre - Centrale-Supélec, Safran

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- *Bran Selic*, Malina SW & Carleton Univ, Canada
- *Safouan Taha*, Supelec, France
- *Masumi Toyoshima*, DENSO, Japan

Publicity Co-Chairs

- *Karima Nahhal*, CEA LIST
- *Jean-Louis Gerstenmayer*, CEA LIST

Architecture Centric Virtual Integration (ACVI 2015)

Friday, June 26th at 9:30

Domain and topics

Cyber-physical have increasingly complex architectures because of the intricacy of the multiple interdependent features they have to manage. They must meet new requirements of reusability, interoperability, flexibility and portability. These new dimensions favor the use of an architecture description language (ADL) that offers a global vision of the system. Due to the even more increased complexity of distributed, real-time and embedded systems, the need for a model-driven approach is more obvious. Models can be used to analyze the system from different perspectives (i.e. latency, scheduling, security, safety). By using models at the earliest in the development process, design issues are discovered earlier in the development process, which would then avoid their propagation across the development process. Using Model-Based analysis would then reduce development efforts and costs while improving system quality.

The purpose of this workshop is to provide an opportunity to gather researchers and industrial practitioners to survey existing efforts related to model-based analysis of cyber-physical systems. Presentations and demonstrations will cover (but are not limited tool) model design, model-based analysis and validation and code generation

Important dates and instructions to authors

Please send your slides (PowerPoint or PDF format) before June, 25 of your presentation to acvi15@easychair.org. Each accepted contribution will be assigned a 30-minute presentation slot including Q&A with the audience. The workshop is also set to encourage discussion between participants during the event, so, please take the presentation as an opportunity to initiate further discussions with the workshop participants. For organizational reasons, you will be asked to use the workshop laptop for your presentation.

Organizing and program committee

Program Chairs

- *Julien Delange*, Carnegie Mellon Software Engineering Institute
- *Peter Feiler*, Carnegie Mellon Software Engineering Institute

Program Committee

- *Agusti Canals*, C-S
- *Etienne Borde*, TELECOM ParisTech
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- *Masumi Toyoshima*, DENSO Corporation
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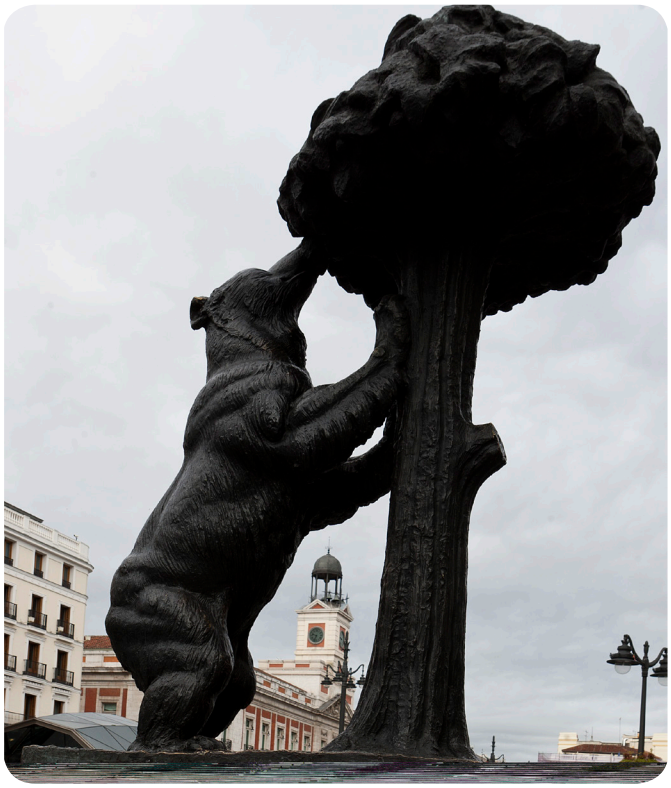
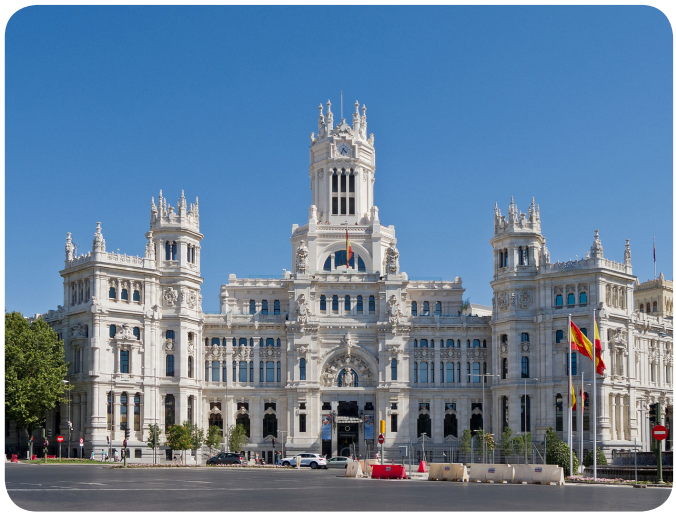
- *Bechir Zalila*, National School of Engineers of Sfax



El oso y el madroño

Intersection of Alcalá and Gran Vía streets



Palacio de Cibeles

Registration

Please access the registration system at http://www.ada-europe.org/conference2015/registration.html

Conference

Early registration cut-off date is June 7th. Lunch is included for every day of the conference that you attend. One banquet ticket is included with 3-day conference registration.

	Members		Non members		Student
	Non academic	Academic	Non academic	Academic	
Early registration	640€	580€	700€	640€	470€
Late registration	700€		760€		510€
Single day registration	350€		380€		N/A

- **Members discount**: Reserved to members of Ada-Europe and members of an "in cooperation with" SIG of ACM (SIGAda, SIGBED, SIGPLAN).
- **Academic discount**: Reserved to full-time faculty members of a university or equivalent educational institution.
- **Student discount**: The conference offers a limited amount of passes under the "student discount" category. This scheme provides full access to all of the conference program, including lunches, banquet, and complimentary proceedings. Access to the tutorials may also be requested. Applicants for this discount should contact the conference chair, providing a copy of a valid student ID. Students that are co-authors of papers accepted for the conference program are eligible for this discount scheme only if at least one other co-author has registered in full.
- **Student waiver program**: The conference this year also features a novel scheme that allows students to access the conference program for free, but strictly without any other benefit. Applicants for this student waiver program should contact the conference chair, providing a copy of a valid student ID. Contingent on logistics, students will be allowed to also apply for this discount scheme directly at the registration desk during the conference, also showing their student ID.

Cancellation policy

Cancellations must be requested in writing. A cancellation fee of 5% will be applied to all cancellations. No refunds will be given for cancellations received after 22nd of May. Substitutions will be accepted.

Tutorials

Lunch is included for full day tutorials, and for two half-day tutorials on the same day.

	Full day	Half day
Early registration	260€	130€
Late registration	290€	145€

Social Program

Welcome Cocktail

Tuesday Evening

The welcome cocktail, after the Ada-Europe General Assembly, will take place at ETSIT-UPM.
AdaCore sponsors this event.

Conference Banquet

Wednesday Evening

On Wednesday evening, the traditional conference banquet will be held at Club de Campo Villa de Madrid, a country club located at the outskirts of the city, with magnificent views. A superb dinner will be served, in a magnificent scenery. During the dinner, the Best Paper Award will also be presented.

Conference Schedule

	Tuesday	Wednesday	Thursday
9:00	Opening / Welcome		
9:30	Keynote Talk	Keynote Talk	Keynote Talk
	IEC-61508 Certification of Mixed-Criticality Systems Based on Multicore and Partitioning Jon Pérez	Software Development of Safety-Critical Railway Systems Javier Rodríguez	The Central On-Board Computer of the Philae Lander in the Context of the Rosetta Space Mission Andras Balasz
10:30	Break & Exhibition	Break & Exhibition	Break & Exhibition
11:30	Regular Session **Language Technology**	Industrial Session **Critical Systems**	Regular Session **Critical Systems**
	Extensible Debugger Framework for Extensible Languages Domenik Pavletic, Markus Voelter, Syed Aoun Raza, Bernd Kolb, Timo Kehrer	Early Experiences in the Industrial Application of SPARK 2014 Angela Wallenburg, Florian Schanda, Stuart Matthews, Alan Newton, Stephen Williams, Neil White	The CONCERTO Methodology for Model-Based Development of Avionics Software Andrea Baldovin, Alessandro Zovi, Geoffrey Nelissen, Stefano Puri
	Static Backward Program Slicing for Safety-Critical Systems Husni Khanfar, Bjorn Lisper, Abu Naser Masud	System Integration in a Railway Setting Theodor Norup	From AADL Model to LNT Specification Hana Mkaouar, Bechir Zalila, Jérôme Hugues, Mohamed Jmaiel
	A Novel Runtime Monitoring Architecture for Safe and Efficient Inline Monitoring Geoffrey Nelissen, David Pereira, Luís Miguel Pinho	Model Based Engineering of an Unmanned Aerial System Jose L. Fernández, Juan López, J. Patricio Gómez	Using Sensitivity Analysis to Facilitate The Maintenance of Safety Cases Omar Jaradat, Iain Bate, Sasikumar Punnekkat
13:00	Lunch & Exhibition	Lunch & Exhibition	Lunch & Exhibition

	Tuesday	Wednesday	Thursday
14:30	Vendor Session	Regular Session **Real-Time Applications**	Industrial Session **Tools at Work**
	Vendor Session	**Schedulability Analysis of PWM Tasks for the UPMSat-2 ADCS** Juan Zamorano and Jorge Garrido **Guaranteeing timing requirements in the IXV On-Board Software** Santiago Urueña Pascual, Nuria Pérez Magariños, Bruno Calvo Chevillat, Carlos Flores Ibáñez **Maintenance of Reliable Distributed Applications with Open-Source Middlewares: Fifteen Years Later** Daniel Garrido and Manuel Díaz	**Multi-Core Testing and Code Coverage** Ian Broster, David George **Deriving Reusable Process-based Arguments from Process Models in the Context of Railway Safety Standards** Barbara Gallina and Luciana Provenzano **Source Code Analysis of Flight Software Using a SonarQube Based Code Quality Platform** Maurizio Martignano
16:00	Break & Exhibition	Break & Exhibition	Break & Exhibition
17:00	Industrial Session **Ada Applications**	Special Session **Advances on Methods**	Regular Session **Multicore & Distributed Systems**
	From Ada 83 to Ada 2012 Philippe Gast and David Lesens **Automated Trading with Ada** Duncan Sands **WCS – Warehouse Control System in Ada** Björn Lundin	**A Task-Based Concurrency Scheme for Executing Component-Based Applications** Francisco Sánchez-Ledesma, Juan Ángel Pastor, Diego Alonso, Bárbara Álvarez **Persistent Containers with Ada 2012** Jacob Sparre Andersen **Effective Worst-Case Execution Time Analysis of DO178C Level A Software** Stephen Law, Andrew Coombes, Michael Bennett, Ivan Ellis, Stuart Hutchesson	**Challenges in the Implementation of MrsP** Sebastiano Catellani, Luca Bonato, Sebastian Huber, Enrico Mezzetti **An Execution Model for Fine-Grained Parallelism in Ada** Luis Miguel Pinho, Brad Moore, Stephen Michell, S. Tucker Taft **AFDX Emulator for an ARINC-Based Training Platform** Jesús Fernández, Héctor Pérez, J. Javier Gutiérrez, Michael González Harbour
18:30	Ada-Europe General Assembly		Best presentation Award / Closing Session
	Welcome cocktail	Conference Banquet / Best Paper Award	

Venue

ETSIT-UPM (*Escuela Técnica Superior de Ingenieros de Telecomunicación, Universidad Politécnica de Madrid*) covers teaching and research in all fields related to Information and Communications Technology, and is one of the leading institutions in that field in Spain. ETSIT-UPM is located in Ciudad Universitaria, the main University campus in Madrid, and can be accessed by metro and bus.

ETSIT-UPM
Avenida Complutense 30
28040, Madrid, Spain
GPS: 40.452886, -3.726183

How to get the ETSIT-UPM

ETSIT-UPM can be reached by bus, metro, or taxi. Bus line F comes from Cuatro Caminos, and bus lines G and 82 come from Moncloa. Both stop at ETSIT-UPM's entrance when coming from Moncloa. However, to take the bus in the return direction you must go to a different bus stop. The metro station Ciudad Universitaria, line 6, is the closest to ETSIT-UPM (1 km away approximately). Moncloa also has a metro station served by lines 3 and 6. Very close to the Ciudad Universitaria station you can connect with bus lines 82, G or U, which stop at ETSIT-UPM.

Connection to airports

ETSIT-UPM can be reached from the Adolfo Suárez Madrid - Barajas airport by taxi, or metro and bus. See the airport web site for more information.

Hotels

The recommended hotel is Hotel Exe Moncloa, which is close to the bus lines G and 82 stops and the Moncloa underground station. There are other hotels in the Argüelles area which are not far from Moncloa.

Hotel Exe Moncloa
Calle Arcipreste de Hita, 10
28015, Madrid, Spain
GPS: 40.433740, -3.717536

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